



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

11/5

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,425	03/22/2005	Yeshaiahu Fainman	0321.68095	9057
<div>24978      7590      05/07/2007</div> <div>GREER, BURNS &amp; CRAIN 300 S WACKER DR 25TH FLOOR CHICAGO, IL 60606</div>				
			<div>EXAMINER</div> <div>RAO, SHRINIVAS H</div>	
			<div>ART UNIT</div> <div>2814</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE</div> <div>05/07/2007</div>	<div>DELIVERY MODE</div> <div>PAPER</div>

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/521,425

Applicant(s)

FAINMAN ET AL.

Examiner

Steven H. Rao

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>01/14/2005</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Priority***

Acknowledgement is made of papers filed claiming priority from PCT/US 2003/022608 filed Jan. 14, 2005 which itself claims priority from U.S. Provisional Application No. 60/397,005 filed On July 18, 2002.

### ***Information Disclosure Statement***

The lds filed on Jan. 14, 2005 has been considered and the initialed copy of the PTO-1449 made of record in the file.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 to 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimura et al. ( U.S. Patent No. 6,684,007, herein after Yoshimura).

With respect to claim 1 Yoshimura describes a method for etching a solid state material to create a surface relief pattern, the method comprising steps of: forming a photoresist layer on the surface of the solid state material ( col. 81 line 39 photoresist over substrate 12) ; holographically patterning the photoresist layer to form a patterned mask ( col. 38 line 60); transferring the pattern in the patterned mask into the solid state material by dry etching.( col.

Art Unit: 2814

26 line 64-65).

With respect to claim 2 Yoshimura describes the method of claim 1, wherein the photoresist comprises SU-8. (col.81 line 39 )

With respect to claim 3 Yoshimura describes the method of claim 1, wherein said step of forming comprises spin coating the photoresist layer.( col. 75 line 52).

With respect to claim 4 Yoshimura describes the method of claim 1, wherein further comprising a step of, subsequent to said step of holographically patterning, optically direct writing a defect into the patterned mask. ( col. 38 line 60, col. 62 lines 21-22, etc.).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

*SA* (5 to 21) Claims 5-21 rejected under 35 U.S.C. 103(a) as being unpatentable over

Yoshimura et al. ( U.S. Patent No. 6,684,007, herein after Yoshimura) as applied to

Art Unit: 2814

claims 1-4 above and further in view of Kumar et al. ( U.S. Patent No. 5,223,356 herein after Kumar) also cite by applicant's in their IDS.

With respect to claim 5 Yoshimura describes the method of claim 4.

Yoshimura does not psecifcally mention wherein said step of holographically patterning comprises: conducting a first volumetric interfering of at least two beams.

However Kumar , a patent from the same field of endeavor describes in col.11 lines 5 to 12 and col. 9 lines 65 to col. 10 line 7 describes conducting a first volumetric interfering of at least two beams, to monitor and maintain desired diffraction efficiency of holographic image obtained by the two beams.

Therefore , it would have been obvious to one of ordinary skill in the art the time of the invention to include Kumar's step of holographically patterning comprises: conducting a first volumetric interfering of at least two beams in Yoshimura's method. The motivation to make the above combination is to monitor and maintain desired diffraction efficiency of holographic image obtained by the two beams ( Kumar col.11 lines 40-50).

The remaining limitations of claim 5 are :

and after changing the position of the solid state material and the photoresist layer, conducting a second volumetric interfering of at least two

beams. ( Kumar col. 11 lines 20-25).

With respect to claim 6 Yoshimura describes the method of claim 4, wherein said step of holographically patterning comprises changing the angle between two interfering beams used in the holographically patterning to introduce a period change in the periodic pattern. . ( Kumar col. 11 lines 20-25).

With respect to claim 7 Yoshimura describes the method of claim 4, wherein said step of holographically patterning comprises changing the exposure time during the holographically patterning to introduce a duty cycle change in the periodic pattern.<sup>39</sup> ( Kumar fig. 6 –graph)

With respect to claim 8 Yoshimura describes the method of claim 4, further comprising steps of: post-exposure baking the photoresist layer exposed by said steps holographically patterning and optically direct writing; and developing the photoresist layer form the patterned mask. ( Yoshimura col. 21 line 2-curing).

With respect to claim 9 Yoshimura describes the method of claim 8, comprising optimizing said steps holographically patterning and post-exposure baking to increase aspect ratios of the mask pattern transferred into the

photoresist layer and to increase the quality of the geometric shape of the mask pattern. ( inherent to optimize the steps).

With respect to claims 10-14 , 16-17 Yoshimura describes . The method of claim 9, wherein optimizing said step of holographically patterning comprises adjusting exposure power per unit surface area, holographically patterning comprises determining an Optimal exposure time preliminary soft baking, performed immediately prior to said step of holographic patterning a sub-wavelength optical structure an optical grating having sub-wavelength spacing between grating elements. ( Yoshimura examples and Kumar examples).

With respect to claim 15 Yoshimura describes the method of claim 8, wherein the exposure power in said step of holographic recording is in the range of 35 to 90mJ/cm<sup>2</sup>. ( Kumar col. 9 lines 40-45) .

With respect to claims 18 and 19 Yoshimura describes the method of claim 1, wherein the solid state material comprises a semiconductor quality Group III-V material layer (18) and GaAs ( cl. 19) ( Yoshimura col. 27 lines 30-35).

With respect to claim 20 Yoshimura describes a spectral filter, comprising: a substrate ( 12) ; a multi-layer structure having layers with alternating refractive indices ( Yoshimura fig. 155-157, etc.); nanocavities etched into the multi-layer structure ( Yoshimura fig.9 # 38) ; and periodic defects (34) in the multi-layer structure interrupting the alternating refractive indices with

Art Unit: 2814

alternating periodically ( periodic defects with alternating periods – well known in the art).

With respect to claim 21 Yoshimura describes a method for forming a photonic lattice pattern in a semi-conductor crystal: forming a photoresist layer on the semi-conductor crystal ( col. 81 line 39 photoresist over substrate 12); exposing the photoresist layer by volumetric interference of at least two beams that create an interference pattern in the photoresist layer to expose a photonic lattice pattern ( Kumar col.11 lines 5 to 12 and col. 9 lines 65 to col. 10 line 7; creating at least one defect in the photonic lattice pattern by optical direct writing ( well known in the art ) : developing the photoresist layer to form a mask ( Yoshimura col. 26 lines 1-20); and dry etching to pattern the semiconductor material and remove the mask. ( Yoshimura col.26 lines 10-15).

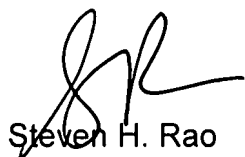
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Art Unit: 2814

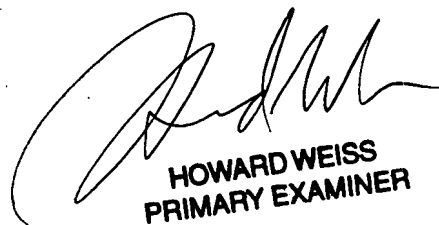
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Steven H. Rao

Patent Examiner

April 27, 2007.



HOWARD WEISS  
PRIMARY EXAMINER